CQ TV

FEBRUARY 1972 **77**

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EDITORIAL

Due to my enforced absence from home, working for a while in Northern Ireland, this issue of your journal is not only late, but smaller than usual. So may I first apologise for this state of affairs and promise you that all will be well in the future. And after all, 26 pages isn't too bad is it? A couple of years ago you were lucky to get 12!

The next C Q - T V will be a real bumper issue as it will precede our next Convention, a bi-ennial event as you probably know. The venue this year will be the ITA Headquarters in Knightsbridge, London, and the date a weekend in September. We'll let you know the exact days in plenty of time. All the usual events - display of members equipment (why not bring <u>your</u> gear along?), lectures on atv topics, the Club General Meeting and of course, the opportunity to meet all those G6s and others who like yourselves, are interested in amateur television.

Only those who have paid their subscriptions can come of course! Last year we stopped sending C Q - T V to 200 "members" who hadn't paid up. You should have heard the howls of protest! So if you intend to come to the Convention, or still want to receive C Q - T V or just want to remain in the Club - send off your subscription renewal NOW. There's a form included with this magazine; use it!

In this issue you will find Part 1 of a series of articles by G6ADK/T Nigel Walker entitled "Ideas for Amateur Colour" Nigel hopes to introduce the theory and practice of colour television in a straightforward manner such that we can all understand the system sufficiently well to build our own equipment, or at least comprehend other peoples' gear. This series will spread over several issues, as the subject is a vast one, but each individual topic will be covered completely in one part. Next time the subjects will be signal decoding together with the amateur colour station.

May I draw your attention to page 24 and the notes printed there on a proposed change to our Constitution. This change will only take place if a majority of members consider it to be a useful change and are prepared to vote that way. So please study it carefully, and at the Club's General Meeting vote the way YOU think things ought to go.

THE EDITOR

CONTENTS

IN THE NEXT CQ-TV

Details of the 1972 Convention.

Colour for the Amateur Part 2.

All the regular articles again.

2nd World SSTV Contest

Sponsored by cq elettronica Magazine

cq elettronica Magazine proposes the 2nd World Slow Scan Television Contest.

The purpose of this Contest is to promote increased interest in the SSTV mode of operation as used by Radio Amateurs.

RULES

1) PERIOD OF CONTEST

1st	15.00 - 22.00 GMT	February 5th, 1972
2nd	07.00 - 14.00 GMT	February 13th, 1972

2) BANDS

All authorized frequencies.

3) MESSAGES

Exchange of pictures and number of the message.

4) EXCHANGE POINTS

a. A two way contact with a station receives one point. (Total points will be the number of individual stations contacted).

b. No extra points for the same station contacted on different bands.

c. A multiplier of ten points for each Continent and of five points for each Country (ARRL list) worked is given.

5) SCORING

Total exchange points times the total of the multipliers.

6) LOGS

Logs will contain date, time, GMT, band, call sign, message number sent and received, points.

7) PRIZES

1st A free 12 month's subscription to cq elettronica Magazine.
2nd A free 6 month's subscription to cq elettronica Magazine.
3rd A free 6 month's subscription to cq elettronica Magazine.

Special SWL prize.

8) All logs must be received by March 20th, 1972.
Send them to:

Professor Franco Fanti
via A. Dallolio 19
40139 BOLOGNA Italy

THE CQ·TV SPG

A TRIPLE STANDARD MONOCHROME SPG using TTL.

by A. W. Critchley Dip El, C Eng, MIERE. **Part 3.**

There have been so many requests for further information about the SPG, and the Mains-locking system in particular, that this third part has been added to what was originally intended to have been a two-part article.

This third (and last ?) part contains some minor corrections and discusses various points about the SPG, its Power Supply and the Genlocking system. There are also details of an improved Genlocking system, a Mains-locking system and a Comprehensive locking system which allows for multistandard Genlocking, Field Superlocking, Mains locking, Field Pulse locking, Crystal Control or free-running.

Errors in previous parts.

CQ-TV 75 page 4 fig.1 N2 pin 5 is shown joined to pins 9 and 13. These should be 8 and 13 as the printed circuit in CQ-TV 76 shows. In fact, neither 8 nor 13 is required to make the SPG work - they are blank pins conveniently used.

CQ-TV 75 page 5. Composite Syncs ...second of the three, five-unit pulses.

CQ-TV 75 page 7 fig.5 waveform B. For N11C read N11B.

CQ-TV 75 page 10, Table. The 405 pulses should be :- 20.25, 39.95, 9.4, 7.9, 1.5, 18, 9.5, 5.5, 4.0, 8.0, etc., from left to right.

CQ-TV 76 page 16. Line Ident, paragraph four. ...high and low on alternate half lines.

CQ-TV 76 page 16. Line Ident. For N13$\overline{BQ}$ pin 8 read N13BQ pin 9.

CQ-TV 76 page 18. 405 UK version. To make it quite clear - R33 and R34 are deleted, D15 and D16 are deleted. N1A pins 1 and 2 need not be connected to anything.

CQ-TV 76 page 22, fig. 12. Pins 9 and 27 are to be linked and not 5 and 27. The text on page 20 is correct.

Further Notes

The printed circuit board for the SPG is available from the author at a cost of £1.75 and is ready-drilled in fibreglass. It is offered more or less at cost price as a favour to members of the BATC and postage would be appreciated.

Various modifications mentioned in CQ-TV 76 have now been incorporated and so the diagram in CQ-TV 76 now differs from the actual board. This diagram is as near an accurate reproduction of the original as could be achieved with the printing processes involved in the production of this magazine.

The cost of building the SPG works out at about £10 but can be cheaper if reject types of IC are used. However, it is difficult to remove dud ICs from the SPG board without damaging the track, so test the ICs first in some simple circuitry.

The SPG takes 330 mA if not terminated. This rises to 405 mA upon terminating all four outputs in 75Ω. The Genlock system adds another 100 mA and the Colour extras some 50 mA. The total current is then about 550 mA at five volts.

There is some 20 mV of 'shash'(-40 dB) maximum when terminated and considerably more when not. No low frequency tilt was measurable. The pulse risetimes are about 15 ns as no form of filter is included to slow them down. A simple filter is described later on in this article.

It is not possible to obtain the CCIR standard of 4-volt pulses into 75 Ω as an 8 volt source is necessary. Some sort of transistor output stage would be required.

The switching system for 405 does not seem to be too clear. Figure 4 in CQ-TV 76 showed the rear view of the standards switch. Pin K should go to the normally open contact for 405 UK. For 405 BQ it should not be wired at all. The normally open and normally closed contacts of the switch may then be either joined together, or pins J and L linked. Also for 405 UK pin E must be joined to pin H. For 405 BQ pin H must not be joined to anything.

These connections will allow the selection of three standards on the switch - 405 UK, 525 and 625 or 405 BQ, 525 and 625.

For 405-only versions R10 and R11 may be combined into one resistor, R10, of 1.3 KΩ. Link A to C then need not be fitted

If the counters are not switched they will count by 7,7,7,9 and 8 for N5 to N9 respectively, giving 3087 lines interlaced with 8 Equalising pulses, 8 Broad pulses and 8 Equalising pulses. The field rate is then about 10 Hz.

The Belgian standard of Line Ident calls for a 5 µs pulse at 7.8 KHz with the leading-edge at Line Sync start. This variation can be obtained by the additional circuitry shown in figure 1. The existing Line Ident square-wave is used to trigger an R-S bistable formed from NOR-gates. The other input to the bistable is Line Drive. The pulse from the bistable is fed to two gates in parallel which

provide a 75 Ω feed. For details of the NOR-gate see CQ-TV 75 page 17.

Fig. 1 System for Belgian Line Ident

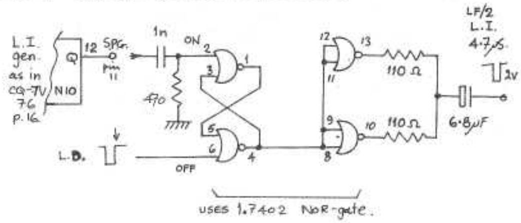
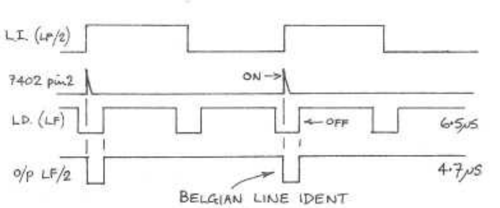


Fig. 2 Waveforms for fig. 1.



The frequency range of the master oscillator has been found to be mainly on the low side. To remedy this R3 should be increased to 2.7 KΩ from 1.8 KΩ. Control of the frequency range is rather coarse and this can be improved by increasing R1 from 6.8 KΩ to 15 KΩ to give a range of ± 6 % (60 to 68 µs). However, if the Genlocking system is to be used it may be as well not to modify this value to allow for a different free-running frequency when the Genlocking system is added. It would, with the improved Genlocking system shortly to be described, be an advantage to bring RV1 out to the front panel on wires as this control then doubles as the Line Phase control as well as the Master Oscillator control.

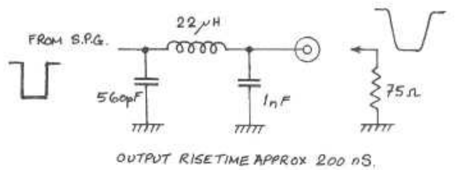
The anti phase-modulation resistor, R44, generally seems to be of the order of 360 KΩ rather than 300 KΩ and the value seems to be fairly critical to set with any great accuracy. Luckily the effect of phase-modulation on normal pictures is slight. Since the setting of the Master Oscillator control alters the value required of R44 for complete cancellation, this control should be centrally placed whilst adjusting R44.

When the Genlock system is in use it is found that the free-running frequency of the Master Oscillator is not the same as it is without the Genlocking circuitry attached. To minimise the difference a 3.6 KΩ resistor should be fitted between the d.c. feed to the oscillator and earth.

A very narrow spike was discovered in the Field Drive output of multi-standard versions of this SPG due to the effects of the stray capacity across D15 and D16 in conjunction with R33 and R34. This spike appears between the first and second portions of this waveform - see CQ-TV 75 page 6, figure 4, waveforms D to G - because the second and third portions are delayed with respect to the first. Normally the spike would not be troublesome and co-axial cables etc. would remove it but when the Mains Locking system (to be described shortly) is used with the SPG then the spike cause problems by falsely triggering a bistable. The cure is to add a 100 pF capacitor from pin K to pin A (earth); this delays the first part of the Field Drive waveform to match the rest.

Figure 3 shows a simple output filter. This π-filter slows down the rise-times of the output pulses to about 200 ns and the output must be terminated if it is used. Normally the ordinary outputs from the SPG are quite good enough for amateur purposes. An inductive type of filter is required in order to try to obtain a Gaussian response i.e. symmetrical, to the edges of the waveforms.

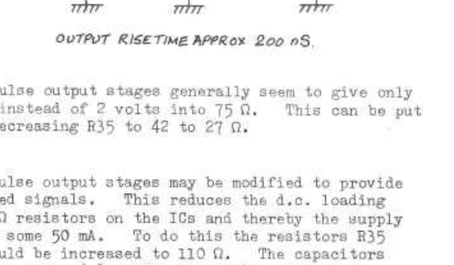
Fig.3. π-section, Low-pass Filter



The pulse output stages generally seem to give only 1.9 volts instead of 2 volts into 75 Ω. This can be put right by decreasing R35 to 42 to 27 Ω.

The pulse output stages may be modified to provide a.c. coupled signals. This reduces the d.c. loading of the 75 Ω resistors on the ICs and thereby the supply current by some 50 mA. To do this the resistors R35 to R42 should be increased to 110 Ω. The capacitors required are then; 6.8 µF for Line Drive, 330 µF for Field Drive, 2000 µF for Blanking and 100 µF for Syncs. These values give a 1 % tilt in the longest part of the waveform so for Amateur purposes smaller capacity values would be satisfactory. For Burst Gate the capacitor is 2.2 µF and the resistors 110 Ω but for Line Ident, because the waveform is a squarewave, the resistors need to be only 68 Ω and the capacitor 47 µF. See also the article on ICs in this issue.

Fig.4 A.c. coupled Pulse Outputs



If the SPG is correctly set for 625 lines, then upon switching to 405 lines the Line Drive becomes 4 µs, Line Blanking 11.3 µs, Line Sync 4 µs and there is no Front Porch - everything else is correct. However, all the pulses can be set correctly by means of the controls. The ranges of these preset controls can be better optimised between standards if the following changes are made :-

Broad Pulses. Decrease C5 from 1 nF to 820 pF.
Front Porch. Decrease R9 from 10 KΩ to 8.2 KΩ.
Line Blanking. Increase C8 from 2.2 nF to 2.7 nF.
Line Drive (& Sy). Decrease R16 from 10 KΩ to 4.7 KΩ.
Equalising Pulses. Decrease R18 from 3.9 KΩ to 1.8 KΩ.

Power Supply

Zener diode stabilisation in the power supply is not as good as it might be because the current through the diode is too low. To increase it, decrease the 8.2 KΩ resistor to 3.9 KΩ and the 270 Ω to 100 Ω. This will improve the zero-to-full-load regulation to ± 0.2 %.

The voltage-setting control gives a range of 4.4 to 5.6 volts. Ripple is about 15 mV (-50 dB). The regulator will function properly only if the input d.c. voltage is greater than some 7.8 volts. This is as measured at the bottom of any ripple across the input smoothing capacitor. The average d.c. voltage therefore needs to be of the order of 9 volts (with 2000 µF or so) and an input of 12 volts is recommended. This may seem to be high compared with the output voltage but the regulator transistors must have a working margin. The 3-volt drop across regulator transistors is often ignored with higher voltage supplies with the consequence that it is forgotten when a low-voltage supply is to be used.

The heat dissipated by the 2N3055 is easily handled by a heat sink of some four inches square in free air, but the SPG box can be used although some master oscillator frequency drift (or Line Phase drift when genlocked) must then be expected.

This regulator has been tested with an input range of 7.8 to 50 volts at greater than ½A and the regulation was ± 1.5 % for this input range, but the normal input maximum is 24 volts because of the amount of heat that the 2N3055 has to dissipate. In any case the transistors are not intended to be used at 50 volts.

Take care that the input smoothing capacitor is adequately rated for the secondary voltage and in particular is physically large enough to handle the high ripple current without overheating.

For those who do not want the bother of making a regulator there is an excellent IC made by SGS-Fairchild. This is the L005TI and is a 5-volt regulator in a TO3 case. It will deliver more than 600 mA with a voltage regulation of 0.1 % and has overload and short-circuit protection. No components are required other than a 10 µF capacitor each side of it for decoupling purposes. The input voltage range is 8 to 20 volts, and the price about £1.2.

Colour Circuitry

Figure 5 shows improved circuitry for the additional colour pulse generators. The control ranges have been altered to give better control and the output stage is now a single gate for Burst Gate. Line Ident, however, is kept with two gates because of the higher power requirements in driving a squarewave into 75 Ω.

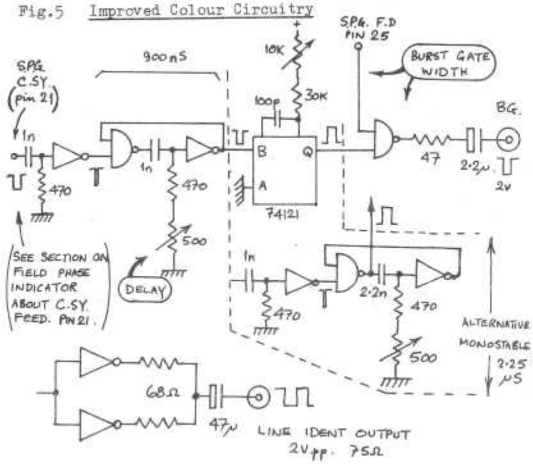
Genlock System as in CQ-TV 76

The two switches were intentionally wired in series so that Field Superlocking could not be performed without also Line Genlocking.

The range of the Line Phase control can be improved by changing the 2.7 nF capacitor to 3.9 nF and the 10 KΩ resistor to 4.7 KΩ. A 3.6 KΩ resistor should be added from the output d.c. oscillator feed to earth.

It may be necessary to increase the input capacitor from 1 µF to 6.8 µF to avoid troubles during the field group period.

Fig.5 Improved Colour Circuitry



In the Superlocking system the 1.5 ms period is in fact 2.2 ms - it has to be longer than the field group period so that only one reset pulse is produced per field by this monostable. The period could be reduced to some 600 ns by decreasing the 220 nF capacitor to 100 nF. However, the system is prone to interference in the form of narrow noise pulses and to reduce this trouble the monostable period should be made even longer - some 15 ms or so. It cannot be made the whole 20 ms otherwise the monostable mistriggers.

The 3.5 µs monostable may be more convenient to make with 4.7 nF and 680 Ω instead of 6.8 nF and 470 Ω.

Some trouble has been found with the bistable being spuriously triggered by interference spikes on the supply and to minimize this the 7473 should be decoupled by 100 nF, or greater, as close to the IC as possible.

The Line Genlock system can be used for 405 if the half-line delay period of the monostable is increased. The actual delay for 525/625 is about 42.3 µs. For 405 it has to be about 115.2 µs (i.e. 98.7 + 18 - 1.5) and so the timing capacitor should be increased to 10 nF.

Simpler Line Genlocking System

The existing genlocking system is inconvenient in several respects - not least because the monostable period has to lengthened for 405 use. If a half-line delayed pulse could be obtained from the SPG directly then there would be no need for the monostable. This can be done relatively easily as figure 6 shows.

To do this, the SPG has to be modified slightly and the details are :-

Delete C13 and its link to the plug pin 7. Join pin 7 to N2Q pin 1 to provide the twice line-frequency pulses which give the timing of Line Sync leading edge.
Break the Line Blanking feed from N14 pins 2 and 11 to the plug pin 13 and instead join the plug to N13B$\overline{Q}$ pin 8. This gives the line-frequency gating with a half-line difference.

These modifications have been done to the printed circuit board supplied by the author but are not present in the layout shown in CQ-TV 76.

Fig. 6 Simplified Line Genlock

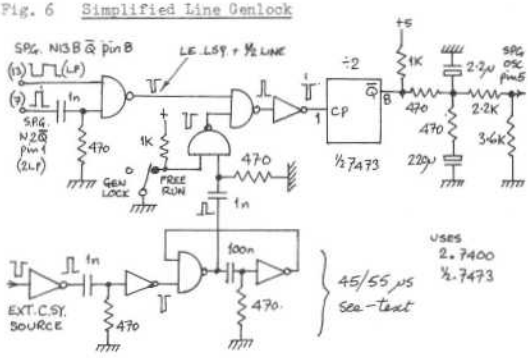
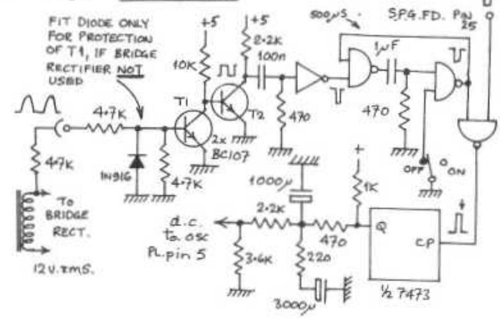


Fig.7 Mains Locking



The interlace bistable N13B determines which of the twice-line pulses forms the line frequency. The unused twice-line pulses do nothing(except during the field group period). It just so happens that these twice-line pulses are half a line out of phase with the ones that are used. Here, then, is a pulse source almost exactly right for the Genlock system. All that has to be done is to make the pulses at line frequency. This is done by using the output of the interlace bistable N13B$\bar{Q}$ pin 8 and a feed of the Broad Pulse gen. N2$\bar{Q}$ pin 1 into a two-input NAND-gate. The output pulse is at line frequency with the timing of the leading-edge of Line Sync plus half a line - whatever the standard. This pulse is used to trigger the bistable directly together with the external line frequency source.

The external Sync source has, of course, got the twice-line pulses in it and these must be removed so as not to upset the line-locking during the field period otherwise a kink will be made in the verticals. They are removed by using a monostable with a period longer than half a line. This monostable is made a simple type in order to take advantage of the fact that with such a monostable when the input period is only a bit longer than the desired monostable period then the output from the monostable is shortened. This happens because the timing capacitor does not have time to fully discharge before the monostable is triggered again. Thus, if the period is set to be greater than half a line on 405 it will reduce somewhat for 525/625 without the twice-line pulses getting through on either standard. The values of figure 6 provide 55 µs on 405 reducing to 45 µs on 525/625. -both greater than a half-line.

There is a snag, of course, and that is that the Broad pulses, being low for a long time, paralyse the input gate of this monostable and the feedback is thus prevented from causing the required snap action during these pulses only. This causes the desired frequency selection of the pulses to go astray. However, this is simply overcome by the use of a differentiating network in the input to the monostable to remove the d.c. effect.

Control of Line Phase is now solely by the Master Oscillator Frequency control and this control should now be brought out to the front panel.

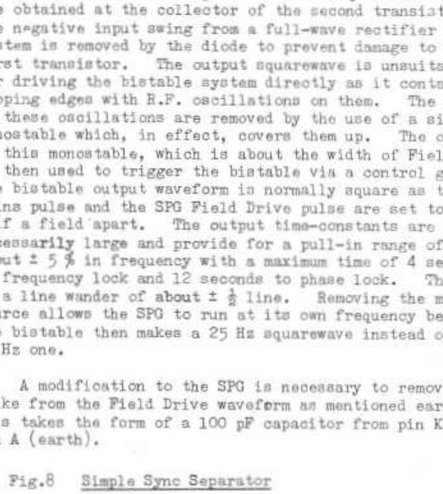
Mains Locking

This can be achieved by modifying the time-constants of the Genlocking system as mentioned in CQ-TV 76 but fig. 7 shows a simpler and better method.

The 50 Hz input from the power supply is used to overdrive a transistor amplifier so that squarewaves are are obtained at the collector of the second transistor. The negative input swing from a full-wave rectifier system is removed by the diode to prevent damage to the first transistor. The output squarewave is unsuitable for driving the bistable system directly as it contains sloping edges with R.F. oscillations on them. The effects of these oscillations are removed by the use of a simple monostable which, in effect, covers them up. The output of this monostable, which is about the width of Field Drive, is then used to trigger the bistable via a control gate. The bistable output waveform is normally square as the mains pulse and the SPG Field Drive pulse are set to be half a field apart. The output time-constants are necessarily large and provide for a pull-in range of about ± 5 % in frequency with a maximum time of 4 seconds to frequency lock and 12 seconds to phase lock. There is a line wander of about ± ½ line. Removing the mains source allows the SPG to run at its own frequency because the bistable then makes a 25 Hz squarewave instead of a 50 Hz one.

A modification to the SPG is necessary to remove a spike from the Field Drive waveform as mentioned earlier. This takes the form of a 100 pF capacitor from pin K to pin A (earth).

Fig.8 Simple Sync Separator



Sync Separator

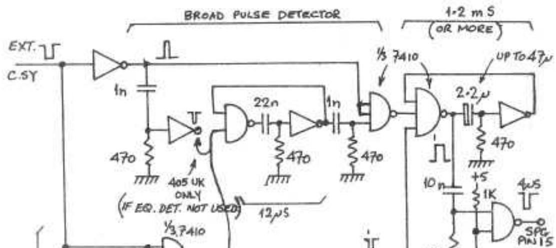
A simple, but effective, Sync separator for use with the genlocking system is given in figure 8. It consists basically of a clipper, T1, followed by an emitter-follower T2. The input biassing resistor is made large so

that the the base current is low and T1 conducts only on the tips of Syncs, i.e. T1 is acting as a d.c. restorer. A pull-up resistor further helps the action with low signal levels. The Zener diode is for protection of T1 only and may be omitted if the input signal never gets greater than 4 volts pp. The second Zener diode is included only to clip off some picture content when the input signal is low. It too may be safely omitted but the input handling range is then worsened by some 6 dB. The 100 pF capacitor is included to remove subcarrier or high frequency noise. The normal input range is ± 12 dB.

Multi-standard Field Superlocking

The present system of Field Superlocking - as shown in CQ-TV 76, page 24 - will not work with 405 UK pulses, or with systems where Field Sync is one long pulse, as, for example, it may be in some cheap industrial TV cameras or Video Tape machines. This is because there are no Equalising pulses to be detected. Some form of a Broad pulse detector is therefore required.

Fig 9. Multistandard Superlock



This is made possible by the use of the circuit shown in figure 9. The presence of a Broad pulse is detected by observing the absence of a Line Sync pulse trailing edge after a given time. For 405 UK this time is some 10 to 40 µs. For convenience in the circuit of figure 9 the period is made 12 µs by the use of a monostable triggered from the leading-edges of Composite Syncs. This has to be done either through a differentiating network or from the output of the 3.5 µs monostable because the simple monostable suffers from poor output pulse shape if the input period exceeds the monostable output period. This is due to the input signal preventing the feedback action from occurring. In this case the output is required during the Broad pulses which are longer than the 12 µs pulse. The 3.5 µs feed is used in this multi-standard version so as to save components.

The output of the 12 µs pulse is differentiated to obtain the trailing edge and this is gated with positive going Syncs so that during **each** Broad pulses <u>only</u>, a pulse is provided at +12 µs. This pulse is then used to trigger the 1.2 ms monostable which, because it has such a long period, makes only one such pulse per field. The leading edge of that pulse is differentiated to form the SPG reset pulse of some 4 µs width - see figure 10.

The previous system of detecting the equalising pulses is also used to provide a second feed to the 1.2ms monostable.

If, therefore, a system with equalising pulses is in use the monostable receives pulses from these equalising pulse trailing edges and also from the broad pulses. All but the first of these pulses is ignored and that one is from an equalising pulse giving correct resetting. On 405 UK no pulses will be generated by equalising pulses, because there are none, and so the first pulse is a broad pulse - at +12 µs. As long as the resetting pulse finishes during the first half line after its start then all will be well.

If 405 <u>with</u> equalising pulses will never be used then the 1.2 ms period may be reduced to 600 ns or so by making the 2.2 µF a 1 µF.

Incidentally, this circuit makes an excellent field sync separator for monitors, etc.; especially for Slow-Scan use when the time constants will need to be greater. The field sync pulse need only occur once in the form of a longer pulse than the line pulses.

The resetting pulse system just described is automatic with any standard. For single standard versions only the appropriate portion of the circuit need be used.

Simple monostables are used throughout because none of the periods involved is particularly critical and so the use of the 74121 is not justified.

Improved Field Superlocking

The present system of Superlocking as just described is susceptible to interference in the form of narrow pulses because of the method of operation of the detection circuitry. If the period of the 1.2 ms monostable could be extended then the interference effects would be rather less. Ideally the period should be 20 ms but this is not possible with a simple monostable as it misfires and causes more trouble than it prevents.

Fig. 10 Improvement

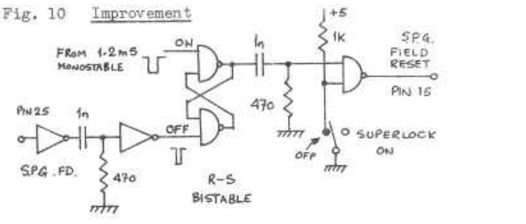
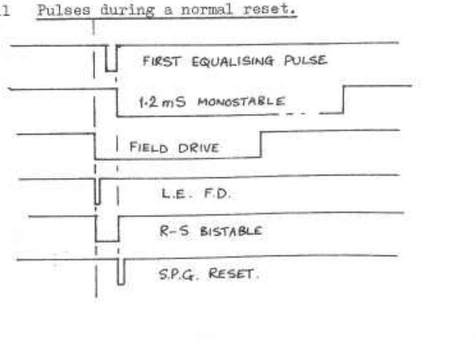


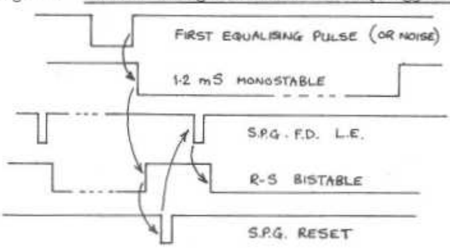
Fig. 11 Pulses during a normal reset.



Another method is therefore employed which uses an R-S bistable. See figure 10. The bistable is set by the first Equalising (or Broad Pulse for 405 UK) as usual, and reset by a pulse as near 20 ms later as can be made by simple means. This particular pulse is in fact the leading edge of Field Drive from the SPG some 19.996 ms later, or 4 µs <u>earlier</u> from the previous field. The bistable thus generates a 4 µs pulse and the trailing edge of this pulse is used to provide the SPG reset-pulse by differentiation. So for 19.996 ms the bistable, and hence the SPG also, is immune from any interference after the first Equalising pulse. During the 4 µs interference can set the bistable and thus make an SPG reset pulse but this pulse will not have any effect on the SPG because the counters, etc., will have just been internally reset and for the next half-line do not change their states, i.e. they are being reset into the state that they are already in, hence, no effect on the SPG. The system is therefore, to all intents and purposes, immune to any interference in the form of pulses.

How then, does it get into the correct phase ? When the external source is first applied, the first pulse to be detected, whether noise or Equalising, sets the R-S bistable and thereby produces a reset pulse for the SPG. This then resets and starts the field sequence. The leading edge of Field Drive then resets the R-S bistable, but now the bistable is left in the opposite state to normal and is thus open to be set by <u>any</u> pulse during the next 20 ms. If this pulse is the first Equalising pulse then the R-S bistable reverts to normal and noise is ignored. If the pulse was a noise pulse then the SPG phase would be set incorrectly and the next field would still be open to resetting pulses. Eventually a first Equalising pulse will get there first and all will be well.

Fig. 12 <u>Pulses during an initial reset (exaggerated)</u>



There are, of course, some snags to this otherwise perfect system. If the external signal starts up with any Equalising, or Broad, pulse other than the first, it is possible for the SPG to remain in this incorrect phase. This is overcome by the use of a long-pulse generator, which could be a 1.2 ms monostable, as before, or an R-S bistable. The problem is how to turn off such a bistable. The answer is to obtain the trailing edge of Line Sync, which does not commence until after the field group period is over. A three-input NAND-gate is used to form this and is fed with the 3.5 µs and 12 µs pulses and differentiated Syncs. The first two pulses create a period from 3.5 to 12 µs which is the only time that the third input can have an effect in. The only trailing edges which occur during this are those of Line Sync. See figure 13. The R-S bistable thus makes a pulse of duration a half-line longer than the field group period. (Any interference at other times during the field results in a pulse which is always less than one line period)

Fig. 13 <u>Forming a long pulse</u>

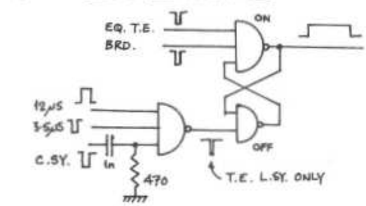
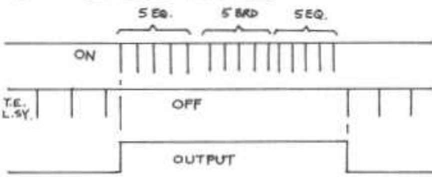


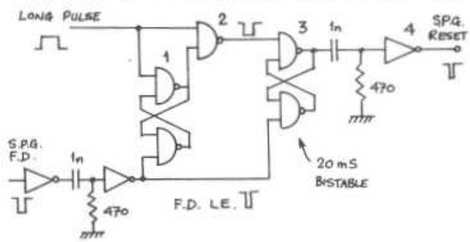
Fig. 14 <u>Forming a long pulse</u>



Because of this pulse, it is now possible for the SPG Field Drive leading-edge pulse <u>not</u> to reset the 20 ms bistable if the Field Drive starts during the long pulse. The long pulse must therefore be differeniated before feeding the 20 ms bistable. The duration of this pulse must be shorter than the one from the Field Drive pulse so that the 20 ms bistable is left in the correct state by the Field Drive input, otherwise the SPG would be prevented from resetting at all.

The need for this critical state of affairs can be eliminated, however, by the use of a third R-S bistable which detects the presence of both pulses and removes the long pulses from the 20 ms bistable thus allowing the Field Drive input to leave the bistable in the correct state. This is shown in figure 15.

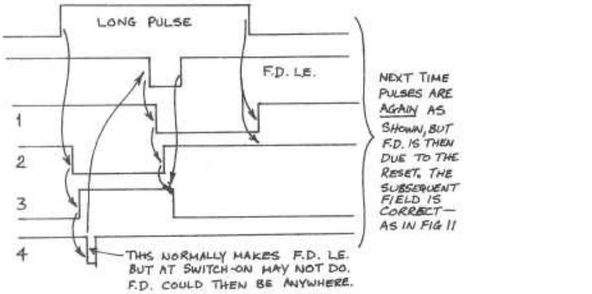
Fig. 15 <u>Removing long pulse from R-S bistable</u>



The output from bistable gate 1 will be high at all times outside the long pulse because this pulse is low. Gate 2 therefore passes the input long pulse to the 20 ms bistable gate 3 which transfers it to the output gate 4 and then to the SPG in the form of a reset pulse.
If the Field Drive pulse starts within the long pulse gate 1 will change state because the long pulse is then high. Gate 1 output will thus go low and gate 2 output will go high. This removes the long pulse low from gate 3 and the 20 ms bistable is allowed to change state because the Field Drive leading-edge pulse is still there.

This situation remains until the long pulse again goes low when the output of gate 2 goes high and so the 20 ms bistable is not affected. The next input pulse will trigger the bistable, however, and result in a reset pulse to the SPG. This pulse may occur before the Field Drive pulse, in which case the SPG changes its field phase to match. It then takes one more field to become immune to interference. If the reset pulse occurs after the Field Drive the SPG is made immune immediately. Figure 16 shows the action.

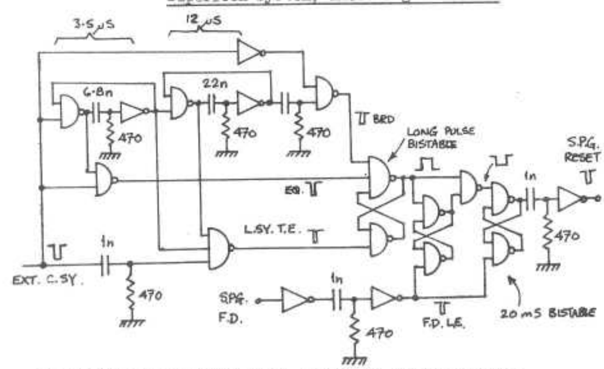
Fig. 16 Field Drive during a long pulse (exaggerated)



This arrangement works very well and the system is stable unless the first Equalising pulse is omitted. The SPG then resets to the next such pulse and on the subsequent field goes back to the correct phase. It may, however, not get back quickly enough to avoid some interference and this results in a slow field roll into the correct phase. This only happens when the interference is heavy and the Line Genlock is on the point of not holding. The effect is like a proper field genlock but only happens in one direction.

The alternative to having this system is to fit a switch on the Superlocking facility and turn it off when the phase is correct.

Fig. 17 Complete system for multi-standard Field Superlock system, including 'lockout'



The combined noise 'lockout' and Broad pulse detection systems enable the Superlocking system to work on 405 UK pulses as well as on 525 and 625 pulses. With a few slight modifications it will work with Slow-Scan systems too, where the vertical sync pulse is one long pulse. Of course the Slow-Scan SPG would have to be a similar type to this SPG. The Broad pulse detector also forms the basis of a Field Sync separator for use in Picture Monitors, etc.

COMPREHENSIVE LOCKING SYSTEM

This system caters for almost every possibility and is shown in figure 18. It looks rather fearsome at first sight but actually consists of the subsections just mentioned together with a common control system.

Line Genlock and Crystal Oscillator source

The Genlock system is basically the same as shown in figure 6 but with the addition of a retriggerable monostable (74123) which is used to detect the presence of the external signal that the SPG is to be locked to. If the signal is not present then the monostable is not triggered and the Genlock source is instead the Crystal Oscillator source - if the control system is selecting Genlock. If this source is also absent then the SPG free runs. The fail-safe to Crystal control is done so that an accurate line frequency can be maintained so that Video Tape Recorders are not upset by the change. Crystal Genlock is available as a mode of operation as is direct Crystal Control of the SPG. The latter is necessary for colour working.

The 45/55 µs monostable is run from the 3.5 µs monostable output in the Superlocking system in order to save having a differentiator and a gate. Two NAND-gates perform the changeover from video to crystal locking, and a bistable is included in the crystal source to provide line frequency pulses. This bistable is not essential as the system will lock to a twice-line frequency source if necessary, but it is better with it.

There is also a changeover system made with a 7450 (or 7451) which selects line, or field,-rate inputs to the Genlocking bistable (7473). The reason for including this changeover is that if the two halves of the 7473 are used for line-rate and field-rate locking at the same time, then the field half interferes with the line half due to the common packaging such that the Line Genlock is modulated by field. This causes 25 Hz sideways flutter of the Genlocked pictures by some ½% or so and is quite noticable. This could be overcome by stopping the action of the field half but the problem then is that the output d.c. would no longer stay at the right value for free-running - and, having long time-constants, it would take a very long time to recover upon switching back to field-rate locking. So, in this case, only one bistable is used and the input source is switched. So, too, is the output after filtering. Both line and field time-constants are permanently attached because it does not matter which polarity of output is used for locking and so both are employed, i.e. Q for line and $\bar{Q}$ for field.

Field Superlocking

Figures 13 and 15 are incorporated into figure 18 with no changes.

Mains Locking

The circuit of figure 7 is employed here with the addition of a 10 ms monostable for Field Phasing ± 6 ms. There is also a changeover system to allow a Field Pulse to be used instead of mains as a locking source. On both of these inputs the long time-constant output from the locking-bistable is selected (see figure 19).

Field Pulse Locking

Here is an alternative field-rate input for use in situations where a mains frequency source may not be available, or when a Telecine machine may provide a field pulse, etc. The field phase control enables the SPG to be brought into perfect synchronism with such a pulse.

Fig. 18

Comprehensive Locking Unit

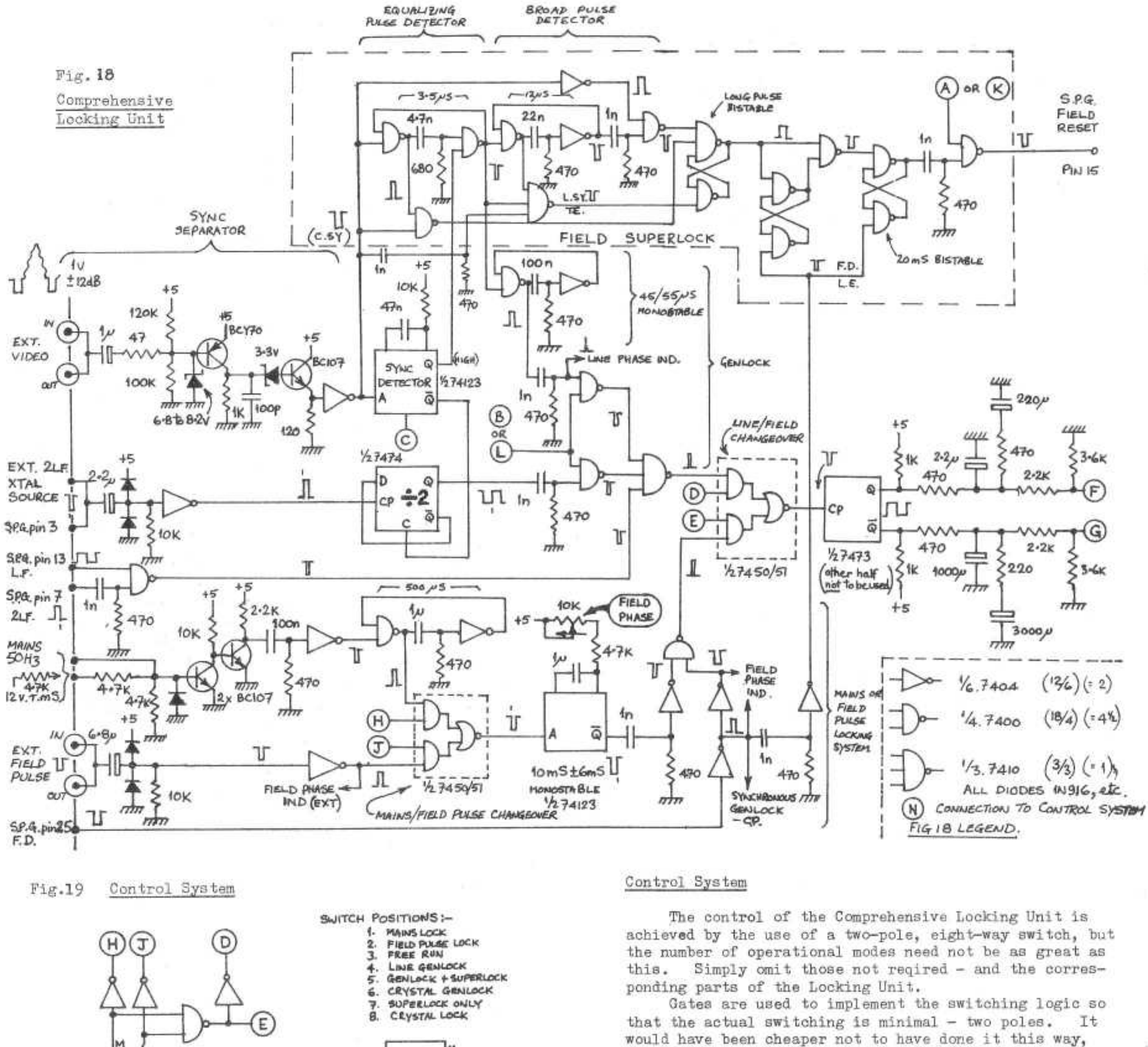
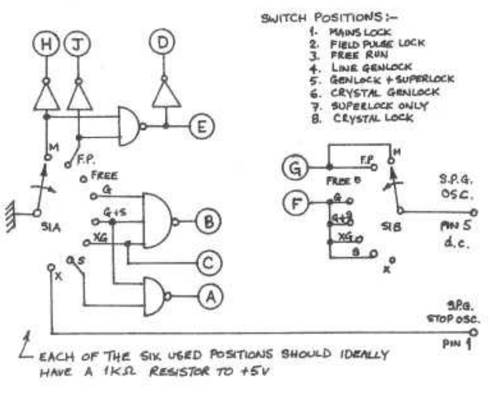


Fig.19 Control System



Control System

The control of the Comprehensive Locking Unit is achieved by the use of a two-pole, eight-way switch, but the number of operational modes need not be as great as this. Simply omit those not reqired - and the corresponding parts of the Locking Unit.

Gates are used to implement the switching logic so that the actual switching is minimal - two poles. It would have been cheaper not to have done it this way, but there would have been a lot of wires and switch poles. As well as being cheaper, it would have been more liable to errors during construction.

Free-running

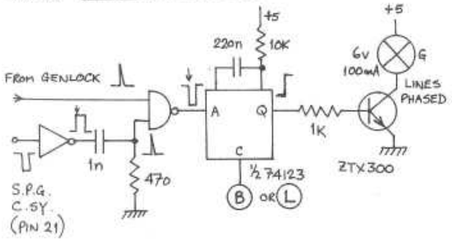
In the free-running state the only parts of the locking system in use are the line-frequency (plus a half-line) and the Genlock bistable. This is done so that the d.c. output remains at about the right voltage to give the free-running frequency although the oscillator is not connected to the voltage. This then gives the least interruption to the SPG upon switching to some other state such as Genlock.

Indication of Phased lines

This is an optional extra and consists of a re-triggerable monostable fed from a NAND-gate. This gate is fed with pulses of about 600 ns width from the two sources of Line Sync leading-edge so that if the pulses are coincident to within ± 600 ns, the monostable is triggered. See figure 20. The monostable output is arranged to turn on a transistor lamp driver.(A 74121 would work, but gives dimmer indication since output is a.c.)

A modification to the SPG board is required in order to be able to get the SPG Composite Sync feed. Break the earth track from the plug pin 21 and instead join pin 21 to N15 pin 6.(SPG earth pins should be 6, 22 & 32)

Fig.20 Line Phase Indicator

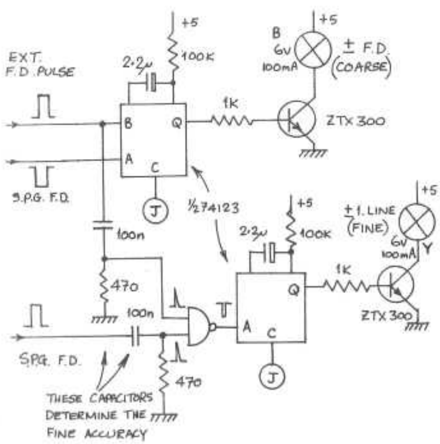


Indication of Field Phasing

A similar method to that of the Line Phase Indicator is used here, except that two indications are provided for fine and coarse phasing. These are to within ± 1 line and ± 7½ lines (on 625). Two are used because Field Phasing is more difficult to set than Line Phase.

The retriggerable monostable is in this case the complete detector for the two wider pulses. See fig. 21

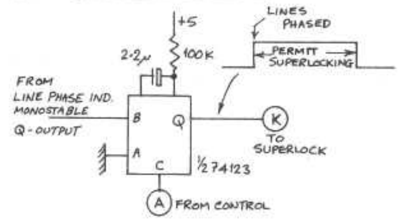
Fig.21 Field Phase Indication



Automatic Superlock pulse removal

This refinement removes the Superlocking pulses after a few have been generated so that interference cannot cause false field resetting. This removal facility is not initiated until the lines are in phase. See fig. 22

Fig.22 Automatic Superlocking

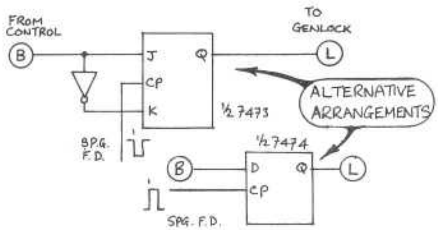


Synchronous Genlock Switching

Figure 23 shows a method of switching in, or out, the Genlock system during the Field Blanking period in order to minimise the visible effects of switching.

The unused half of the 7473 J-K bistable can be used in this application but the 7474 does the job rather better.

Fig.23 Synchronous Genlocking - Two Methods.



Printed Circuit for Genlock/Colour Board

This board will shortly be available from the author for £1.75 plus postage. It contains provision for all of the features of the locking systems described in this article. Not all of them need be incorporated, of course, but the provision is there if required.

The board is of the same general style as the SPG board and has the same dimensions. There is a small front panel.

Conclusions

The SPG and its associated locking systems have been proved to be satisfactory in their performances for Amateur use and also for some professional Industrial Installations.

The complete installation represents a considerable saving in cost over a professional SPG with a performance not markedly inferior. The small size and low power consumption make it ideal for mobile applications.

The SPG and its locking systems were intended to be put together in the form of blocks with the minimum of interdependance and in this respect the design is quite flexible.

Acknowledgements

The author wishes to thank the Directors of EMI Electronics Ltd. for permission to publish this article.

A Multiburst Generator

D. J. Long G6ACH'T

Where it is important for an amplifier to have a particular frequency response, it is usual to achieve this by "frequency-sweeping", a process whereby individual tones are applied to the input of the equipment and the output measured, a series of results being noted down. These results are then used to draw a graph known as a frequency response.

In television it is possible to perform this lengthy operation much more quickly by applying the tones consecutively along a television line, and ensuring that each tone has the same amplitude; a white bar is used as a low frequency reference. At the output of the equipment the response can be immediately seen as an oscilloscope. The waveform is known as "multiburst" and is shown in Fig. 1.

The Master Oscillator (T1 and $\frac{1}{4}$ 7400) oscillates on 3.3MHz and is divided down to six times line rate; other outputs are obtained from along the divider chain. The 5MHz comes from another oscillator locked to 3 times the 1.6MHz output. The Ring Counter clocks around so as th sample all the frequency bars, and white and line blanking, at six times line rate. The combined outputs are obtained from an 7430 8 input NAND gate.

The $\frac{1}{4}$ 7400 feeding the Ring Counter clear inputs is to make sure that the counter only works with one '1' state going through.

Sync is obtained by first narrowing the pulse from the line blanking period then differentiating the result and clipping. The two extra $\frac{1}{4}$ 7400 were to tidy up the edges of the sync waveform.

The whole generator was built on a small piece of paxolin with the I.C.s stuck legs uppermost, and the circuit conventionally wired from pin to pin.

The second -2 of the Master Oscillator i.e. 3.3MHz to 1.6MHz was used, as with -3 the mark/space ration was not 50:50, and so the 0.5 MHz output had to have the -2 after the -3. Some adjustment of the sync forming values may be necessary to achieve ideal pulse widths with

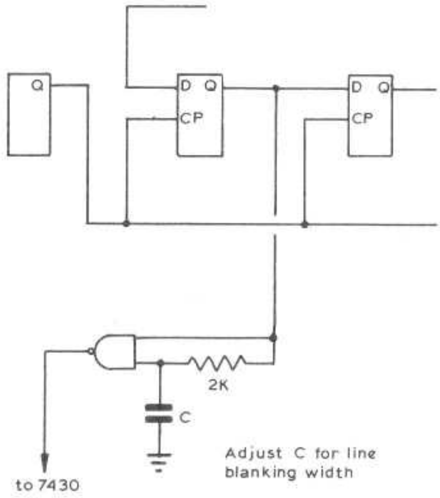


Figure 2 Line Blanking Delay

different I.C.s Line blanking is the interval divided by 6, which is a bit short; this does not matter as it is, after all, only a test signal! However, if the correct timings are required it is possible to delay the start of the white bar by adding another $\frac{1}{4}$ 7400 (see Fig. 2).

Sources of supply for the I.C.s were New Cross Radio (Oldham Road, Manchester) for the 7400, 7474, and 7430 at 5p each, and Bi-Pak for the 7476.

The unit has brought to light some interesting facts about the authors equipment, including his 'scope!

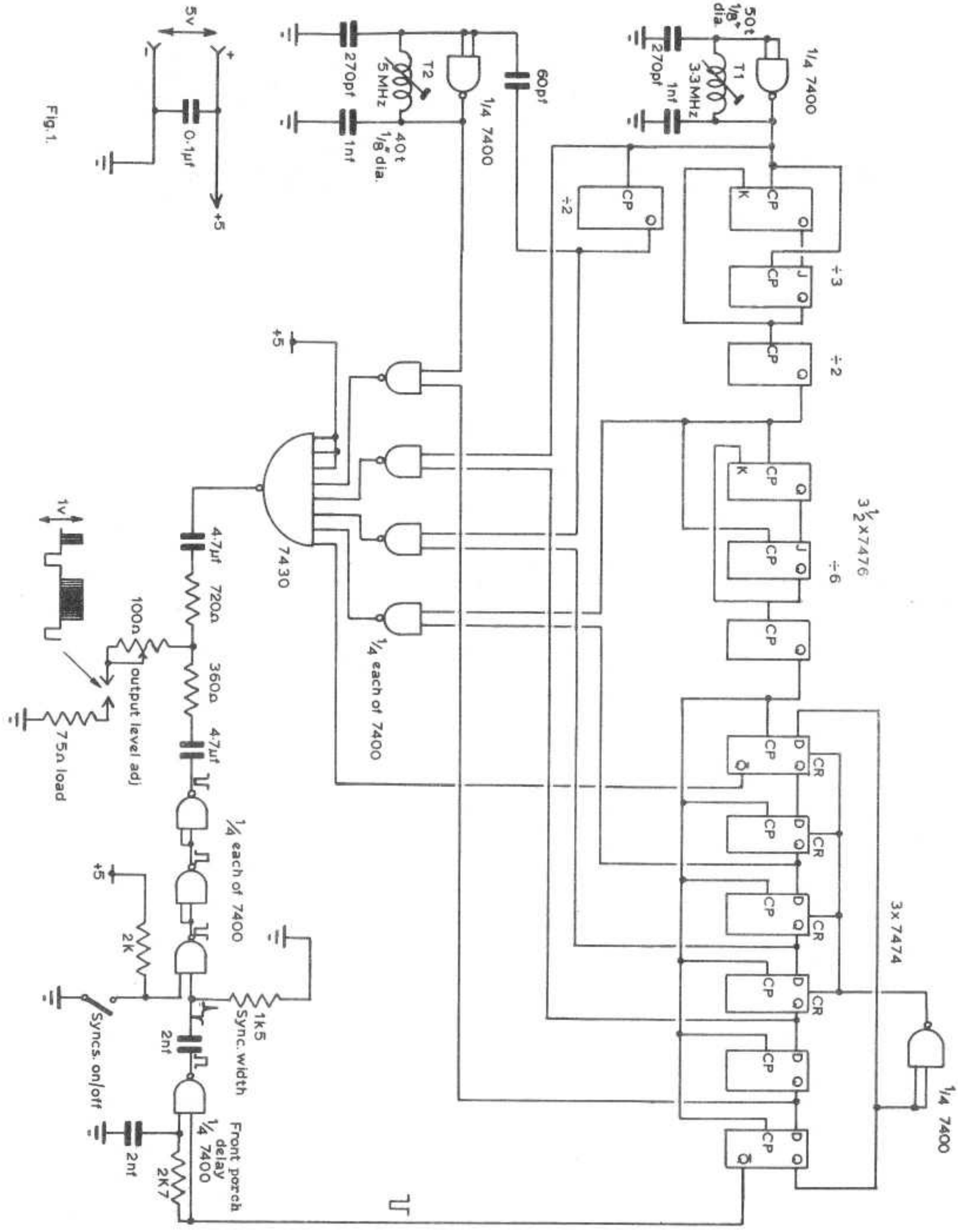

1/4 7400
50t
1/8" dia
T1
3.3MHz
270pf
1nf
T2
5MHz
40t
1/8" dia.
60pf
÷2
÷3
CP
K
J
Q
3½x7476
÷6
3x7474
CR
D
7430
1/4 each of 7400
+5
5v
0.1µf
4.7µf
720Ω
360Ω
100Ω
output level adj
75Ω load
1v
1k5
Sync. width
2nf
2K
Syncs. on/off
Front porch delay
1/4 7400
2K7

Fig. 1.

Ideas for Amateur Colour

Part 1

Nigel Walker
G6ADK'T

There are probably quite a few amateurs who are interested in colour, but do not do anything due to lack of available circuits, or they may think that colour would be impossibly complicated and expensive. It is the purpose of this series of articles to give an indication as to what is involved in the reception and transmission of standard 625 PAL colour.

BASIC REQUIREMENTS

As you all know, to produce a monochrome television picture, you produce all the necessary timings with the four standard outputs from an S.P.G. Well, for colour two additional pulse feeds are required, namely - burst gate and pal switch.

Burst gate is a 2 volt p-p -ve signal which gates the subcarrier to produce a burst of about 10 cycles of subcarrier duration within the back porch period. B.G. (burst gate) starts 5.6uS after the leading edge of line sync and has a duration of 2.5uS. The bandwidth of the burst should correspond to that of the rest of the chrominance signal. More will be said about this later.

P.S.(pal switch) is a 1 volt p-p, 1:1 square wave which occurs at half the line frequency; when fed to appropriate circuitry, it shifts the phase of R-y subcarrier through 180 degrees on alternate lines.

Another feed required is a 1 volt p-p sine wave at subcarrier frequency (4.43361875MHz). For broadcast purposes this frequency has a set relationship to line frequency, this is done to produce subcarrier patterning which has the least objectionable effect on the picture. This relationship is rather complicated, so for amateur purposes the subcarrier can be initially derived from a "free running" crystal oscillator. One way to achieve the relationship would be to receive a broadcast colour, and genlock the S.P.G. to the signal.

ENCODING

Fig. 1 shows the block diagram of a PAL coder. This processes inputs of red, green and blue together with syncs to produce a composite signal; the signal is just like a monochrome one except that there is subcarrier "sitting" on the vision, the p-p amplitude defining the saturation(amount) of colour.

'Y', the luminance signal, is a full bandwidth signal which defines the brightness of the picture, exactly the same as in monochrome. It is obvious that whatever colour an object is it will reflect some light (think about monochrome cameras), so the luminance signal must be derived from proportions of red, green and blue. If you look at different coloured objects through your monochrome camera, you will find that some colours will appear brighter than others. Unfortunately the red will look darkest due to the response of the vidicon tube, it will, however, be seen that the green objects, are much brighter than the blue. Thus the luminance signal is made up of differing proportions of red, green and blue.

The actual equation is:

$$Y = 0.587g + 0.299r + 0.114b$$

Matrix 1 adds the red, green and blue inputs in these proportions to obtain the Y signal.

Matrix 2 subtracts Y from R and B to produce the two colour difference signals - (R-Y) and (B-Y).

The low pass filters reduce the bandwidth of the colour difference signals to that corresponding to the bandwidth of the chrominance signal, which 1.3MHz 3dB points.

The two modulators are the balanced type which produce a double sideband, suppressed carrier signal. It can be seen that the modulators are fed with subcarrier in quadrature (ie. 90 degrees phase difference). This means

that when the outputs are combined, they form a signal whose phase defines the hue of the colour (varying the ratio of the two components will give any phase of signal through 360 degrees), and whose amplitude defines the saturation of the colour (the bigger the modulating voltage, the bigger will be the modulated output). It can now be seen why colour difference signals are used to modulate the subcarrier since, when there is no colour, R=Y and B=Y, so (R-Y) and (B-Y) = 0. Therefore no subcarrier will be present on the signal, and hence no patterning will be visible. The 180 degree switch is another balanced modulator fed with P.S., this therefore reverses the phase of the R-Y component on alternate lines.

The 8.86MHz filter removes the predominately second harmonic distortion from the outputs of the modulators.

Syncs are added to the luminance signal which then passes through a delay line, after which the chrominance signal is added to form the complete encoded signal. Finally, the complete signal is fed to a low pass filter (Bandwidth = 6MHz) to attenuate the intermodulation products in the signal.

The chrominance passes through restricted bandwidth circuits and is thus slowed down relative to the luminance, therefore the luminance has to be delayed as shown.

This series will be continued with Part 2 in C Q - T V 78.

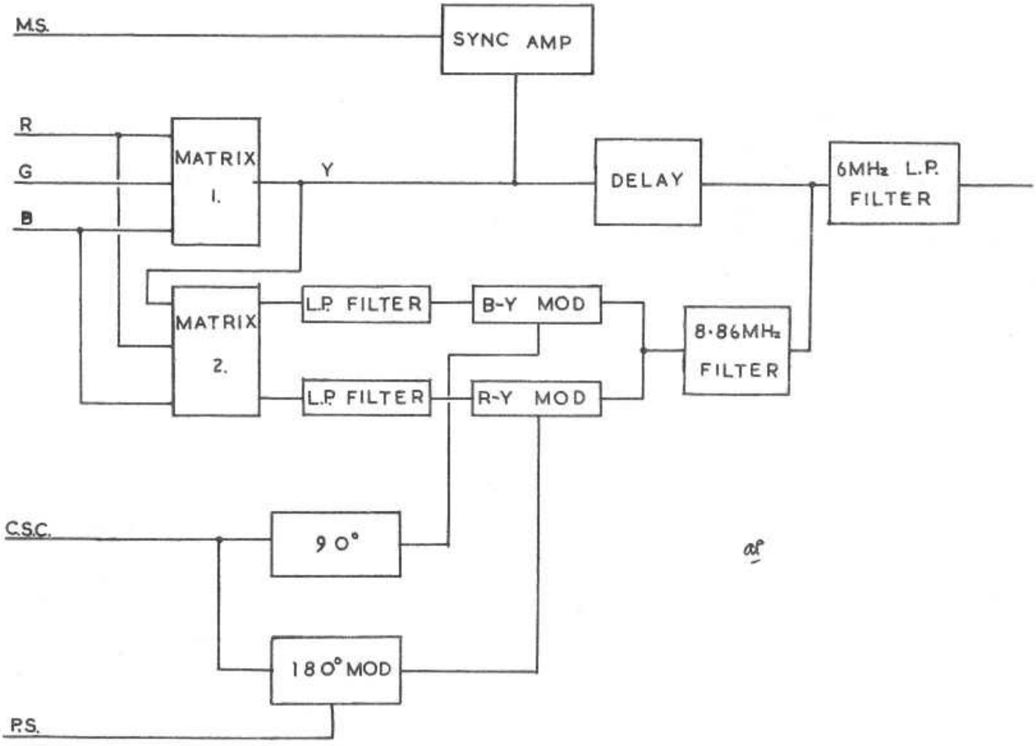


Fig. 1 Block diagram of PAL coder
NOTE: burst producing stages not included.

INTEGRATED CIRCUITS

PART 7.

A.CRITCHLEY Dip El; C Eng; MIERE.

Part 7 Standard Pulse Input and Output Circuitry, a Beam Switch for Oscilloscopes and Push-Button Memory Circuits.

This seventh part in this series on ICs was to have discussed the uses of shift registers and memories but, due to the length of the third part of the SPG article and the reduced size of this issue of CQ-TV, it has been decided to postpone these until the next issue of the magazine. Instead details are given about circuitry for handling standard 75 Ω pulses, a beam-switching unit for an Oscilloscope and push-button memory units.

Standard SPG Pulses

Outputs

Nearly all television equipment has to drive, or is driven by, other equipment by means of standard pulses. These are the usual Line Drive, Field Drive, Mixed Blanking, Composite Syncs and, in the case of colour, Burst Gate and Line Ident. (the latter two being sometimes known as Burst Flag, Y-axis switch, PAL switch, etc.)

In the UK, and many other countries also, these pulses have been standardised at 2 volts peak-to-peak negative-going into 75 Ω, so as to feed co-axial cables.

This is very convenient as far as TTL ICs are concerned because a 75 Ω source when not terminated produces 4 volts - and so does a TTL gate.

Theoretically then, a TTL gate can have 75 Ω hung on it to give 2-volt pulses, but in practise this is not so because the d.c. conditions of the IC are upset. It is, however, possible to overcome the problem to some extent as was described in CQ-TV 73, page 11-12. Figure 1 shows a suitable solution and this has been used in the CQ-TV 75 SPG.

The problem with this method is that two gates are necessary and the output is always above earth. If a series capacitor were included then the d.c. would be removed and so would the excessive loading on the gate. This system does in fact work quite well and figure 2 shows how it is achieved. Values for C and R are given in table 1.

A series resistor is necessary because the output impedance of the gate is less than 75 Ω and thus the source impedance is made up to 75 Ω. Unfortunately, the gate is still upset to some extent by having such a low load resistance to drive and the value of the resistance depends on the type of pulse and its polarity.

The d.c.-blocking capacitor value is determined by the amount of 'tilt' allowable in the waveform at the load and table 1 gives capacitor values for a 1 % tilt. It will be seen that the amount of standing d.c. also depends upon the type of pulse.

The capacitors are rather large for the longer duration pulses as may be expected as the circuit is of course our old friend the differentiator. For amateur use, therefore, the larger values can be reduced to something more convenient without undue effect - unless the following units do not clip the pulses!

Inputs

External pulse sources were also mentioned in CQ-TV 73 and chief amongst these are the standard SPG pulses. The circuit of figure 4 shows the input arrangement necessary to accept standard pulses and table 2 gives the value of C for normal and reduced (double-terminated) input levels.

The 10 KΩ resistor sets the input bias for the IC to make the input normally high in order to accept negative-going pulses. The value of C depends on the amount of tilt that can be tolerated (see fig. 5). Excessive tilt causes the gate to turn off too soon and high frequency oscillations may occur during the mid-point of biassing towards the end of the pulses. Table 2 gives also the maximum value of C that it is necessary to use to avoid any oscillations. Normally the input signal can be reduced to about one quarter of the normal pulses before such oscillations occur. Too large a value of C is expensive, but it should be remembered that if an input arrangement as shown comes after a TTL output stage, also having a capacitor, then the two amounts of tilt will ADD. In general, then, the biggest possible capacitors should be used.

Outputs using two gates

Two gates in parallel to drive a 75 Ω load are

better than one gate alone - for the ICs anyway - the d.c. conditions are less severe. When a series capacitor is used, then the values of the series resistors become higher than when no capacitor is present. This is because the d.c. loading is different. We have just seen this for the single-gate output stage, but when two gates are used for standard pulses the values of the resistors remain constant for each type of pulse. (With the exception of Line Ident which, because it is a square wave, is more demanding.) Figure 6 gives all the details for two-gate outputs.

Fig.1. 75Ω Outputs - d.c. coupled

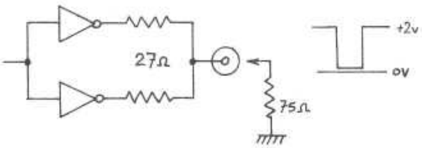


Fig.2. 75Ω Outputs - a.c. coupled - single-ended

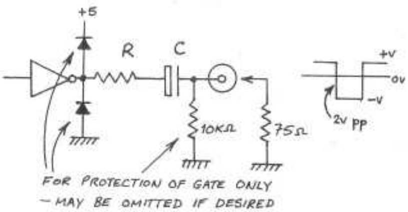


Fig.3. Tilt

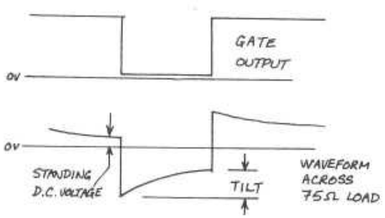


Fig.4. 75Ω Inputs

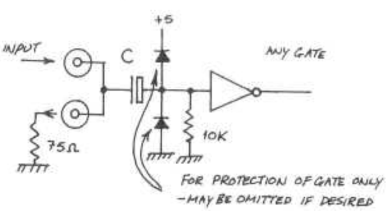


Table 1. 75 Ω Outputs - Values of R and C for 1 % tilt on longest part of pulse

625 Pulse	Longest Pulse μs	Series R Ω	Minimum C μF	Standing d.c. mV
L.D.	6.5	43 or 39	6.8	+ 205
F.D.	480	47	330	+ 55
M.Bl.	1600	24 or 22	2000	+ 565
C.Sy.	27.3	47	100	+ 150
B.G.	2.25	47	2.2	+ 40
L.I.	64	Nil	47	+ 975
(Output on Line Ident is only 1.95 Volts)				

Table 2. 75 Ω Inputs - Values of C to give clean output pulses

625 Pulse	C 2V Pulses	C 1V Pulses	Max C necessary
L.D.	10 nF	22 nF	220 nF
F.D.	470 nF	1 μF	6.8 μF
M.Bl.	32 μF	68 μF	150 μF
C.Sy.	100 nF	220 nF	1 μF
B.G.	6.8 nF	10 nF	100 nF
L.I.	470 nF	1 μF	2.2 μF
(Input resistor for Line Ident 1.8 KΩ not 10 KΩ)			

Fig.5. Oscillations in pulses due to tilt

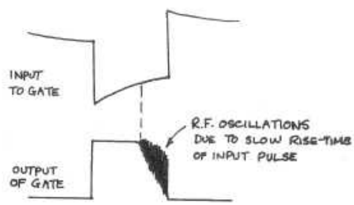
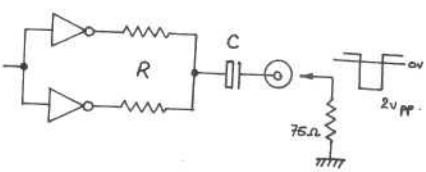
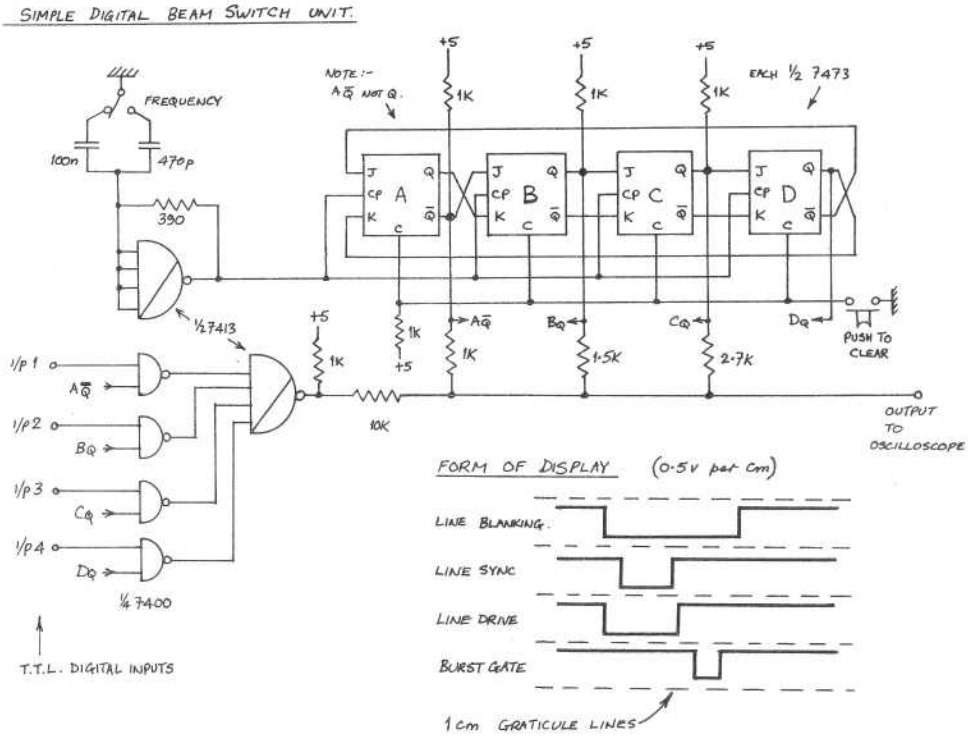


Fig.6. 75 Ω Outputs a.c. coupled - double-ended



The value of C is as shown in Table 1.

The value of R is 110 Ω for L.D., F.D., M.Bl., C.Sy., and B.G. and is 68 Ω for L.I.



SIMPLE DIGITAL BEAM SWITCH

The problem of comparing several digital pulses for relative timing is forever occurring in IC work, especially in Television and in particular when SPG pulses are being investigated. The following circuit provides a simple method of displaying up to four DIGITAL waveforms simultaneously on any oscilloscope - digital only, because digital IC gates are used for ease of construction.

The principle is to rapidly switch between the four signals and at the same time to add a particular amount of d.c. voltage to each of the signals. This d.c. is in effect a Y shift voltage to separate the four traces.

The four input signals are selected by means of two - input NAND-gates and collected together in a four-input NAND-gate. The selection pulse comes from a ring counter (or shift register). This is arranged to provide a high output from only one bistable at a time, by means of the clearing and cross-coupling arrangement. When the bistables are cleared they are all made Q-low but the cross-coupling ensures that the A$\bar{Q}$-output 'high' is fed round the rest of the bistables as a 'high' - one at a time. This provides the circulating selection pulse. The system has to be first cleared otherwise the waveform fed round depends upon what was in the bistables. A push button provides the simplest way of ensuring that the system is cleared properly.

The repetition frequency must not be locked in any way to the input signals and so a free-running oscillator is used to provide the clock pulses for the ring counter. Its frequency is not critical but is usually about 10 KHz. A choice of frequency enables any pulse frequency to be viewed without trouble.

Four different d.c. levels are obtained from the ring counter by means of the 1 KΩ, 1.5 KΩ and 2.7 KΩ resistors to the output point. Note that the $\bar{Q}$ feed of 'A' is used and the Q feeds of 'B' and 'C'. Bistable 'D' is not used and so its d.c. is zero. The selected pulse also goes to the output point via a 10 KΩ resistor which makes its level at the output smaller than the steps between the d.c. levels. Pull-up resistors of 1 KΩ are fitted to the outputs of these feeds to ensure flat d.c. levels.

The output waveforms fit between four adjacent 1 cm graticule lines when the input sensitivity of the 'scope is 0.5 volts per centimetre. Number one input is at the top and so on down to number four.

The oscilloscope must be triggered from an input source - not the oscillator. Note that because the output signal levels are much lower than the normal logic levels it is especially important to decouple the circuitry properly in order to minimize spikes and rings. It should also be borne in mind that the output pulse shapes do not necessarily represent the input shapes because of the amplitude limiting of the gates, although the durations should not be affected to any great extent.

PUSH-BUTTON MEMORY CIRCUITS

Mechanically latching push-buttons are falling out of fashion these days in Television. Instead, electronic memory systems are being used. There are many ways in which the selection of a push-button can be memorised and one of them is by means of digital integrated circuits. The following pieces of circuitry show some simple means for doing the job.

One problem with normal push-buttons is that the contacts 'bounce'; that is, they make and break several times in rapid succession for both making and breaking actions of the switch.

Fig 7 Simple latching push-button memory.

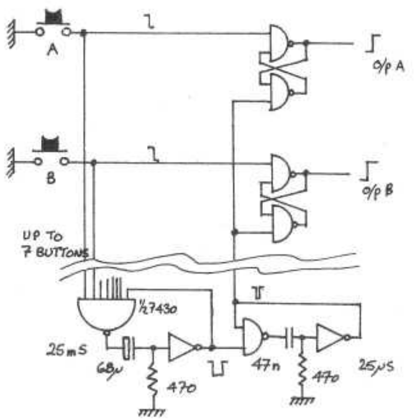
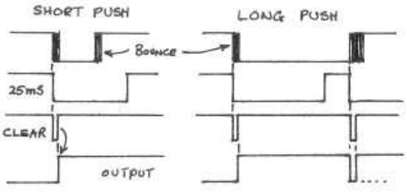


Fig 8 Waveforms for Fig 7



In the first system shown in figure 7 the bounce is overcome by the use of a monostable which produces a 25 ms pulse from the first of the bounce pulses and thus covers-up the rest. Any one of the push-buttons starts this monostable. It also sets an R-S bistable, but whilst it does so, the leading edge of the 25 ms pulse is used to clear all the R-S bistables via a 25 µs monostable. The input due to the pushing of the button lasts longer than this clearing pulse and so just one of the bistables remains set - the selected one. The time periods involved are not critical and represent a compromise between a spikey output signal and a long period between pushes. Both outputs from each bistable have these spikes. There is also another disadvantage with this simple system and this is that more than one button can be pressed at one time and can result in more than one output at once.

Fig 9 Spike-free memory system.

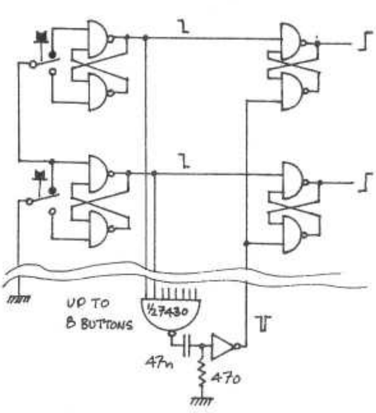


Fig 10 Waveforms for Fig 9.

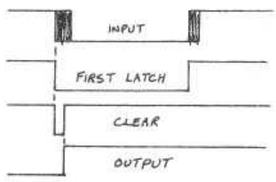


Figure 9 shows a version without output spikes. In this, the input signals are taken from R-S bistables run from change-over push-buttons. These are set and reset by the first bounce and do not respond to further pulses to their inputs once set or reset. The 25 ms monostable is no longer required.

Vision Mixing equipment goes a step further with the switching of video in that the switching time is arranged to always occur during the field blanking time so as to reduce the visible effects of a video cut. This is relatively easy to do with ICs as figure 11 shows.

The buttons are linked to prevent more than one output being selected at once and every button triggers an R-S bistable. The reset input of each of these bistables is fed with the trailing-edge of Field Drive. The output of each bistable thus never exceeds one Field in duration and always ceases with a Field Drive pulse trailing edge. A two-input NAND-gate follows each bistable and one of the two inputs is Field Drive complete and positive-going. Thus for one button pressed, one of these gates provides a negative-going Field Drive pulse which triggers both a 25 µs monostable and another R-S bistable. This part of the system is then as shown in figures 7 and 8. The output signals change with the leading-edge of Field Drive.

Figure 12 shows an electrical method of providing an interlock. It is intended to fit in the circuit of figure 11 at the points 'X'. The action is very simple. Initially each gate input is low and all the cross-coupled outputs are high because each gate output is high. The first input to go high causes that gate's output to go low and since every gate is connected to every other gate, all the others remain high and cannot be made low. An invertor is then required to get the necessary polarity. Incidentally, this circuit forms the basis of a panel game priority selection system - the first to press the button wins and locks out his opponents.

Fig 11 Switching during Field Blanking time.

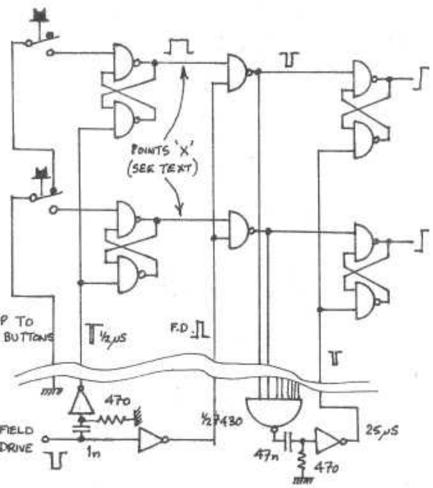
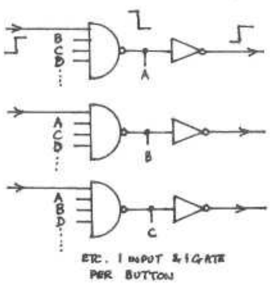


Fig 12 Interlock using gates. (POINT X IN Fig 11)



Corrections and additions to previous parts

Part 6 (CQ-TV 76):-

Figure 5. If C is 1 nF the pulsewidth is 300 ns, for 10 nF it is 2.5 µs.
Note: The input pulse must be longer than the output pulse desired by about three times.

Figure 10. With the values given, the time for recovery is 10 ms which may not be long enough for some switches - increase the 1 MΩ resistor to suit. The pulse width is about 1 µs. The circuit works more reliably if the values are changed to 1 MΩ, 22 nF and 470 Ω. This gives pulses of some 2 µs width with a 40 ms recovery time. The trailing edge of the pulse with either system has a slope.

Figure 13. 47 nF gives 25 µs and the formula should be approximately 500 ns/nF

Figure 14. 2.2 nF gives 14.5 µs

Figure 16. The 39 nF is better as 47 nF and the 1.5 µF as 1 µF, but both values are alright as shown.

Figure 17. There is a timing error in B and C. The 120 µs monostable is triggered by positive-going edges and so the start-time should be at the trailing edge of the pulse shown and not the leading edge. Similarly, the trailing edge of the waveform shown in B and C should start from the trailing-edge of the input pulse after the 45 µs arrow.

Figure 18. The top monostable timing capacitor value is correct at 2.2 nF but the lower one should be 470 pF

Figure 20. There is a timing error in the 120 µs waveform. It should start at the leading edge of the pulse above it. ($\frac{1}{2}$-line earlier)

Acknowledgements

The Author wishes to thank the Directors of EMI Electronics Ltd., for permission to publish this series of articles.

References

CQ-TV 71 to 76 for IC articles.

CQ-TV 75 to 77 for a TTL SPG and Genlock system.

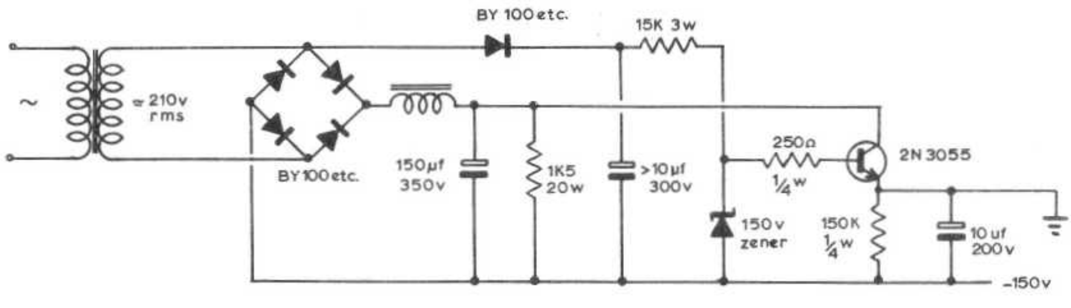
Modulator Power Supplies.

FURTHER NOTES ON THE G6OUO/T MODULATOR
by Brian Kennedy G6AGT/T

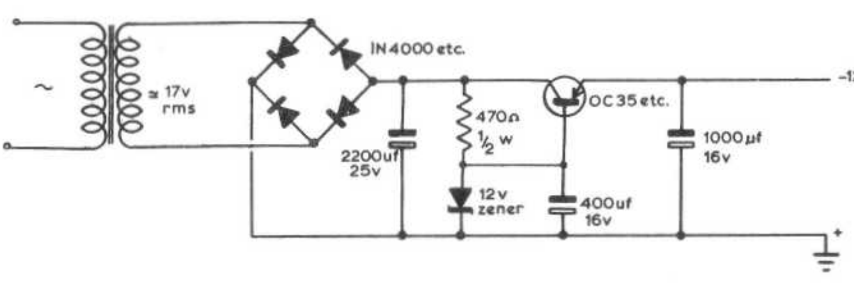
The modulator designed and developed by Dave Mann G6OUO/T and John Ware G6RSA/T and published in C Q - T V 60 required a power supply producing the slightly unusual rails of -12 volts and -150 volts. The circuit below was therefore developed, in conjunction with G6SDB/T, in order to provide the modulator with its own permanent power supply.

Whilst no originality is claimed for the circuitry, it does work well with the modulator, giving very acceptable results and is presented here in case it may be of some use to members who were contemplating construction of the modulator but were stuck for a suitable power supply.

150v stabilised power supply unit



12v stabilised power supply unit



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Members wishing to contribute material for publication are asked to note the following details.

Articles may be type or hand written, and should be no longer than 1500 words; if longer, they should be divided into separate parts.

Drawings or diagrams should be in black ink on white paper 10 inches wide up to a maximum depth of 14 ins.

Photographs should be semi-matt EN-print or postcard size.

Articles are invited on all subjects, in particular those of amateur constructional interest. Please send your material to the Editor C Q - T V (address on page 1) in a stout cardboard backed envelope. Material will only be returned if requested.

POSTBAG

May I thank those of you who sent Christmas cards very much indeed for your kind thoughts.

Brian Kennedy G6AGT/T of Stourbridge who designed the power supplies printed on page 22 has written to say how indebted he is to David Taylor G6SDB/T for his help in preparing the circuits. May we thank you both for letting us have the results of your work.

R. M. Russell G3MGC of Stroud, Gloucester was so lavish in his praise of C Q - T V when he wrote recently that we were quite embarrassed! Thanks for your support, OM; and it's nice to know that not everyone resents the subscription increase. G3MGC is yet another S S T V enthusiast - you will all be outnumbering the fast scan people if you increase at this rate!

Peter Whitton of Manchester should by now be a member (if the form we sent him got through the Christmas rush!) and is building, like many others, the C Q - T V SPG. He hopes at sometime in the future to build a telecine channel to go with his vidicon camera, and he has already built a vision mixer. Good luck with all your projects, Peter.

Eric Cheer of Chichester in Sussex has spent some time building up his dual standard CCTV system, and for a self confessed "newcomer" seems to have done very well. He has built the equipment into two 19" racks using commercial, ham and home-grown gear. There is a valve SPG, a VHF oscillator two monitors (a 17" and a 14") and a vidicon camera using hybrid circuitry. Eric has had some trouble winding coils for this camera to suit his valve circuit and would be grateful for some help, if anyone nearby could assist.

John Tanner G6NDT/T now living in Andover announces that he is back on the air on 70cm. Our stalwart ex-secretary has reappeared with 100 watts vision and has been received already by several members. Welcome back John !

Martin Allard GAEM/T of Brentwood, Essex has sent a note which should prove useful. Mullard varicap UHF tuners are now available and, most important, they will tune down to 70cm. without modification. They have very good noise figures as well. Thanks for the gen, Martin.

H.A.A. Grimbergen PAOLQ of Leiden in the Netherlands wrote to us at Christmas wishing all members the seasons greetings. Glad you look forward to C Q - T V so much OM. PAOLQ enclosed some details of his RTL logic PAL sync generator and test waveform generator. The master oscillator runs at 4MHz and the colour subcarrier frequency is also controlled directly by the M.O. Sounds a good design.

STOP PRESS

The provisional date for the 1972 Convention has been set as Saturday September 16th. More details, including a registration form, will be published in the next issue of C Q - T V.

B A T C COMMITTEE

Mr. A. Moore has offered his resignation from the Committee due to pressure of work. We wish to thank Adrian for his work whilst serving as a member for the last two years, since his election at CAT-70.

ERRATA

In the "I.C. Character Generator" by G6ABE/T in C Q - T V 74 the inputs to the DTL binaries were shown as the JK terminals. When using TTL (e.g. the 7476 I.C.) it should be noted that the 'Set' and 'Clear' terminals should be used. We apologise for any confusion this omission may have caused to members building this unit.

CLUB CONSTITUTION

Item Six of the current Club Constitution reads as follows;

"The Committee of the Club shall consist of the Officers of the Club, namely, the Chairman, Secretary, Treasurer and Editor, (all of which are honorary appointments), together with not more than five elected members. All committee members shall retire at each General Meeting and be eligible for re-election."

As it stands at present this paragraph of the Constitution, if applied to the letter, can only restrict the expansion and smooth running of the Club, as at present the committee work of the Club is being shared by some fourteen members. Your committee therefore recommends that Item Six of the Club Constitution should be amended to read as follows;

"The Committee of the Club shall consist of the Officers of the Club, namely, the Chairman, the Secretary, the Treasurer and the Editor C Q - T V, together with any others the Committee shall deem necessary (all of which are honorary appointments), together with not more than fifteen elected members. All officers and committee members having been in office for two sessions (i.e. approximately four years) must retire, but shall be eligible for re-election. The Committee shall have the power to co-opt members of the Club to serve as officers or as committee members, but all such co-opted members shall be required to retire at the next General Meeting. A minimum of half of the officers and half of the elected members shall retire at each General Meeting."

During the next General Meeting of the Club, which will be held at the 1972 Convention, members will be asked to vote for or against this amendment. Your committee hope that you will approve of the change which recognizes the growth which has taken place within the Club, and whilst maintaining a democratic position it will enable your committee to plan more for the future by removing the requirement for the whole Club Administration to retire en bloc at every General Meeting.

Any member who does not have a full copy of the Club Constitution may obtain one by sending a stamped addressed envelope to the Club Chairman (address on page 1) together with any comments or further ideas which you may have.

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COVER PHOTO

Signals received off air from G6NOX/T Jeremy Royle at CAT-70, the last BATC Convention held at Cambridge. This year's Convention will be held in London.

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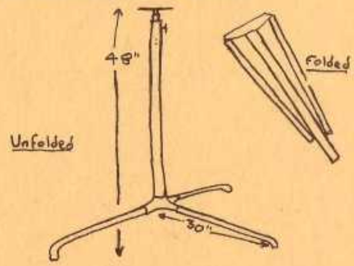

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